IN THE SPECIFICATION

Please amend paragraph [0007] on page 2 of the Specification as originally filed as follows:

Although useful, Flash memories have disadvantages. One disadvantage is ~~th~~ the time required to erase flash memories is considerable, thus limiting their fields of application.

Please amend the paragraph [0032] on page 6 of the Specification as originally filed as follows:

SAS etching is then carried out in a manner known to those of average skill in the art, the result of which is illustrated in FIG. 3. The non-masked zone, corresponding in large part to the zone 71 for the formation for the source line, is etched in this way. The substrate is then dug out under the level of the stack, as shown in discontinuous lines in FIG. 3. Etching can be undertaken in a manner known to those of average skill in the art with products such as CF4 or CHF3. The etching stage likewise partially attacks the protective resin ~~19~~ 14, which creates a deposit of polymers 15 in the hollow below the stack.

Also, please amended paragraph [0036] on page 7 of the Specification as originally filed as follows:

During subsequent stages lateral insulation walls 17 of the cells are formed using any appropriate material. A layer of dielectric material ~~19~~ 18 is also formed according to a mask, so as to receive the cells. Then, in a manner known to those of average skill in the art a bit line 19 is created in contact with respective drains 8. The section of FIG. 6 is made along a bit line 19, after formation of the latter.